Advanced 3D monolithic integration in Myfab/Electrumlab - the example of Ge transistors

Scaling and new materials has allowed the most advanced integrated circuits today to contain over 10 billion transistors on a die of about 5 cm^2. The critical dimensions of the transistors are in the 10-20 nm range and continued increase of the device packing density is core to continue Moore's law. Economics and/or physics might eventually stop continued scaling and a possible route to increase packing density would be to stack transistor on top of each other, so called monolithic 3D integration. In this talk I will describe the challenges and opportunities for monolithic 3D integration and in particular describe our research on Ge MOSFETs for monolithic 3D integration. I will also describe the infrastructure for Integrated Circuit fabrication at the Department of Electronics.